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Integrated 1D epitaxial mirror twin boundaries for ultrascaled 2D MoS_2 field-effect transistors

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In atomically thin van der Waals materials, grain boundaries—the line defects between adjacent crystal grains with tilted in-plane rotations—are omnipresent. When the tilting angles are arbitrary, the grain boundaries form inhomogeneous sublattices, giving rise to local electronic states that are not controlled. Here we report on epitaxial realizations of deterministic MoS_2 mirror twin boundaries (MTBs) at which two adjoining crystals are reflection mirroring by an exactly 60° rotation by position-controlled epitaxy. We showed that these epitaxial MTBs are one-dimensionally metallic to a circuit length scale. By utilizing the ultimate one-dimensional (1D) feature (width ~0.4 nm and length up to a few tens of micrometres), we incorporated the epitaxial MTBs as a 1D gate to build integrated two-dimensional field-effect transistors (FETs). The critical role of the 1D MTB gate was verified to scale the depletion channel length down to 3.9 nm, resulting in a substantially lowered channel off-current at lower gate voltages. With that, in both individual and array FETs, we demonstrated state-of-the-art performances for low-power logics. The 1D epitaxial MTB gates in this work suggest a novel synthetic pathway for the integration of two-dimensional FETs—that are immune to high gate capacitance—towards ultimate scaling.

Hexagonal transition metal dichalcogenides possess a threefold rotational symmetry[1–5], and during monolayer (ML) crystallization they often form mirror twin boundaries (MTBs) as one-dimensionally extended line defects within the host lattice, where two adjoining ML crystals are reflection mirroring with 60° in-plane rotation[6,7]. Although the usual kinds of grain boundary (GB) in ML transition metal dichalcogenides, where the in-plane tilting angles are random[8–11], have long been regarded as unwanted crystallographic defects, this MTB was identified to be particularly intriguing in that its band dispersion linearly intersects the Fermi level of the host lattice to establish genuine one-dimensional (1D) electron systems, as predicted by density functional theory calculations of MoS_2 (refs. 9,12–15) and $MoSe_2$ (refs. 16–19). These electronic states were also characterized to be 1D Tomonaga–Luttinger liquid[15,18–20] or 1D charge density waves[21–23] by scanning tunnelling microscopy and spectroscopy investigations at low temperatures. However, so far, experimental verifications of the 1D electronic states have been done on MTB segments a few nanometres long that were accidently crystallized in ultrahigh vacuum conditions.

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Thus, their full potential as unique 1D metals for practical utilizations has not been explored. In this work, we report a synthetic route to fabricate scalable MoS_2 MTBs and their networks to an electronic circuit level by deterministic van der Waals (vdW) epitaxy and verify their metallic properties as robust 1D ohmic conductors at room temperature with a simple d.c. measurement at both individual and network levels at large scales[24]. As a proof of concept, we integrated these 1D MTBs as an atomic-scale gate to construct vdW heterostructure field-effect transistors (FETs) in both individual and array FETs towards ultimate size scaling.

MTBs imbedded in MoS_2 ML bicrystals

Epitaxial growth of MoS_2 ML bicrystals was established by coherent bicrystal stacking of threefold MoS_2 MLs on sixfold *c*-plane sapphires (Fig. 1a,b). Within this stacking framework, one can expect two crystallographic variants of MoS_2 hexagon in the initial nucleation stage[25], which were 60° rotated from one to the other, as indicated with blue and red triangles in Fig. 1a. As the growth proceeds (Fig. 1b), these hexagon nuclei form triangular facets with S-terminating zig-zag edges, under S-rich growth conditions (Supplementary Fig. 1)[26], that is, the S-terminating zig-zag edges of MoS_2 MLs are aligned perpendicular to the <11$\bar{2}$0> orientation of *c*-plane sapphires, resulting in two triangular variants that are equally favourable in their formation energy[27,28]. Then, when these two variants coalescence, they can form 60°-rotated GBs, sharing the S-terminating zig-zag edges. In our S-rich growth condition, each facet edge is predominantly S-terminated, from which we can naturally assume that the MTB sublattice is S-edge sharing (4|4E)[15]. Note that here we use nomenclatures of the *a*|*b* defect, which refers to the dislocation core composed of *a*-fold rings and *b*-fold rings in the hexagonal system surrounded by a perfect network of hexagons[29]. Thus, the 4|4E GB sublattice, in which each S chain along the GB is reflected with the half-unit cell slip, is composed of fourfold rings sharing the edge (Fig. 1c)[9]. We have achieved MoS_2 ML bicrystals using our metal–organic chemical vapour deposition (MOCVD) in a near-equilibrium growth regime as shown in Fig. 1d,e, where we maintained a slow lateral growth rate <0.5 μm min^{-1} by controlling the flow rate of Mo sources with low partial pressures ($p_{Mo(CO)6} \approx 10^{-6}$ torr) (see also Supplementary Fig. 2). Statistically, two crystal facets occur at 50:50 populations, maintaining the threefold in-plane rotational symmetry, as in Fig. 1d (see also Supplementary Fig. 3). This ensures that the imbedded GBs within the MoS_2 ML host lattice are always MTBs and no other 1D sublattice (Fig. 1e), as also verified with a low-energy electron diffraction pattern (Fig. 1e, inset) of the two threefold variants. A cross-sectional image obtained by bright-field scanning transmission electron microscopy (BF-STEM) shows that two MoS_2 variants are seamlessly stitched in a <10$\bar{1}$0> orientation, forming the MTB, as indicated with orange squares in Fig. 1f. Here, the MTB can be determined as a transition point between two variants, distinguished by the bond directions between the darkest spots representing Mo columns with their nearest neighbouring S columns. Using dark-field transmission electron microscopy (DF-TEM), our MTB textures of the 60° GBs can be visualized, as shown in Fig. 1g (also see Supplementary Fig. 4 and Supplementary Note 1 for more details). Moreover, it can be visualized after selective-etching the GBs by water vapour[30] (Supplementary Fig. 5). The exact definition of the imbedded MTB networks at the 60° GBs is discussed in Fig. 1h–k, where it contains straight MTB segments (Fig. 1h) and zig-zag MTB segments (Fig. 1i) with the 60° kinks. Whether the 1D MTB is straight or zig-zag is simply determined by mutual orientations of two adjoining facets during the coalescence, which can be either a rhombus or a bow-tie, as discussed in more detail in Supplementary Fig. 6. The straight MTBs, which can be extended over a few tens of micrometres, are always 4|4E (S-edge sharing), as confirmed with two S atoms between Mo atoms along the line intensity profile in Fig. 1j,k. The width of the 4|4E sublattice at the MTBs is ~0.4 nm. Near the exact 60° turn at the kinks, where one or two Mo vacancies are present[31], the 4|4P sublattice (S-corner sharing) is locally observed, while the 4|4E sublattice is still a majority component (Supplementary Figs. 7 and 8).

Figure 2a shows the current (*I*)–voltage (*V*) characteristics of a line MTB channel contacted with Ti/Au (Fig. 2a, top left inset), in comparison with a single-crystal MoS_2 ML (MoS_2 S-ML) channel, clearly showing substantially lower resistance (*R*) of 10–100 kΩ μm^{-1} at room temperature (see also Supplementary Fig. 9). Here, note that, because our epitaxial MTBs are imbedded in the MoS_2 bicrystals, one cannot technically measure the intrinsic *R* of the MTBs (R_{MTB}) as an individual resistor. Rather, we estimate it by measuring the *R* of the MoS_2 bicrystal channels containing the MTBs, which is the parallel resistor of the imbedded MTB line and the host MoS_2 S-ML (R_{MoS2}). In that, the R_{MTB} must be even lower (see Supplementary Fig. 10 and Supplementary Note 2 for estimation of the R_{MTB} considering the contact resistance). In fact, the line MTB is a robust conductor, capable of carrying currents up to tens of microamperes at room temperature (Fig. 2a, bottom right inset), similarly to metallic single-walled carbon nanotubes a few micrometres in length[32]. The metallic character of the MTBs is also evident in ($R_{MTB} + R_{MoS2}$) variation at low temperatures in Fig. 2b, where the ($R_{MTB} + R_{MoS2}$) slightly increases at lower temperatures (the sheet resistance (R_S) < 10 MΩ per square at 5 K), while the R_{MoS2} exponentially increases, as expected for a typical band semiconductor, exceeding the R_S of 10^4 MΩ per square at 5 K (see Supplementary Fig. 11 for the corresponding *I*–*V* characteristics and the estimated R_{MTB} as a function of temperature). Furthermore, the transfer characteristics of the FET with an MTB channel exhibit very weak gate-voltage dependence; it also verifies the metallic nature of the MTB (Supplementary Fig. 12). Visual evidence of 1D metallicity was captured by conductive atomic force microscopy (C-AFM) at room temperature, where the current map verifies the continuous conducting pathways through the 1D MTB networks, including the straight MTB lines and 60° kinks (Supplementary Figs. 13–15 and Supplementary Note 3). These 1D metal network textures can be modulated with adjusting the average grain sizes by growth kinetics controls (Methods); the denser networks with smaller grain sizes provide higher numbers of 1D metal pathways with higher connectivity. Figure 2c is the variation in the R_S of bicrystal channels (8 μm long and 50 μm wide) at 5 K, whose average grain lengths (G_L) range from 6 to >40 μm. Indeed, we found that the R_S substantially decreases by five orders of magnitude in the smaller-G_L bicrystals, following a percolation pattern in the R_S–$1/G_L$ plot. This 1D percolated metal network is also manifested in the temperature-dependent R_S, where the denser network exhibits a typical metallic behaviour (Fig. 2d and Supplementary Figs. 11 and 16).

Designing scalable MTB networks

The fact that the scalable 1D metal networks can be hosted by epitaxial growth suggests exciting opportunities to realize a new type of two-dimensional (2D) circuitry. To this end, we attempted to grow our bicrystals by position-controlled epitaxy. Figure 3a shows such an epitaxy schematic, where we patterned small dots on *c*-plane sapphire substrates by Ar ion milling to be served as nucleation seeds. We have achieved one-to-one correspondence between each dot and a crystal facet. By lithographically defining the dot patterns, one should be able to construct diverse 1D network geometries with the bases of the straight line and the 60° turns. Figure 3b shows growth demonstrations of these geometrical arrangements, that is, a single line, a 60° kinked line, a zig-zag line and parallel lines, with the corresponding second harmonic generation (SHG) mapping images, which can identify the locations of the 1D MTBs within the host lattices. Note that the presence of dark lines at the MTBs is attributed to destructive interference of the SHG signals from the adjoined crystals, where the destructive interference is maximized when the adjacent crystals are rotated by 60° (ref. 33). It is remarkable to visually verify the scalable MTB networks up to a scale of a few tens of micrometres by designed vdW epitaxy.

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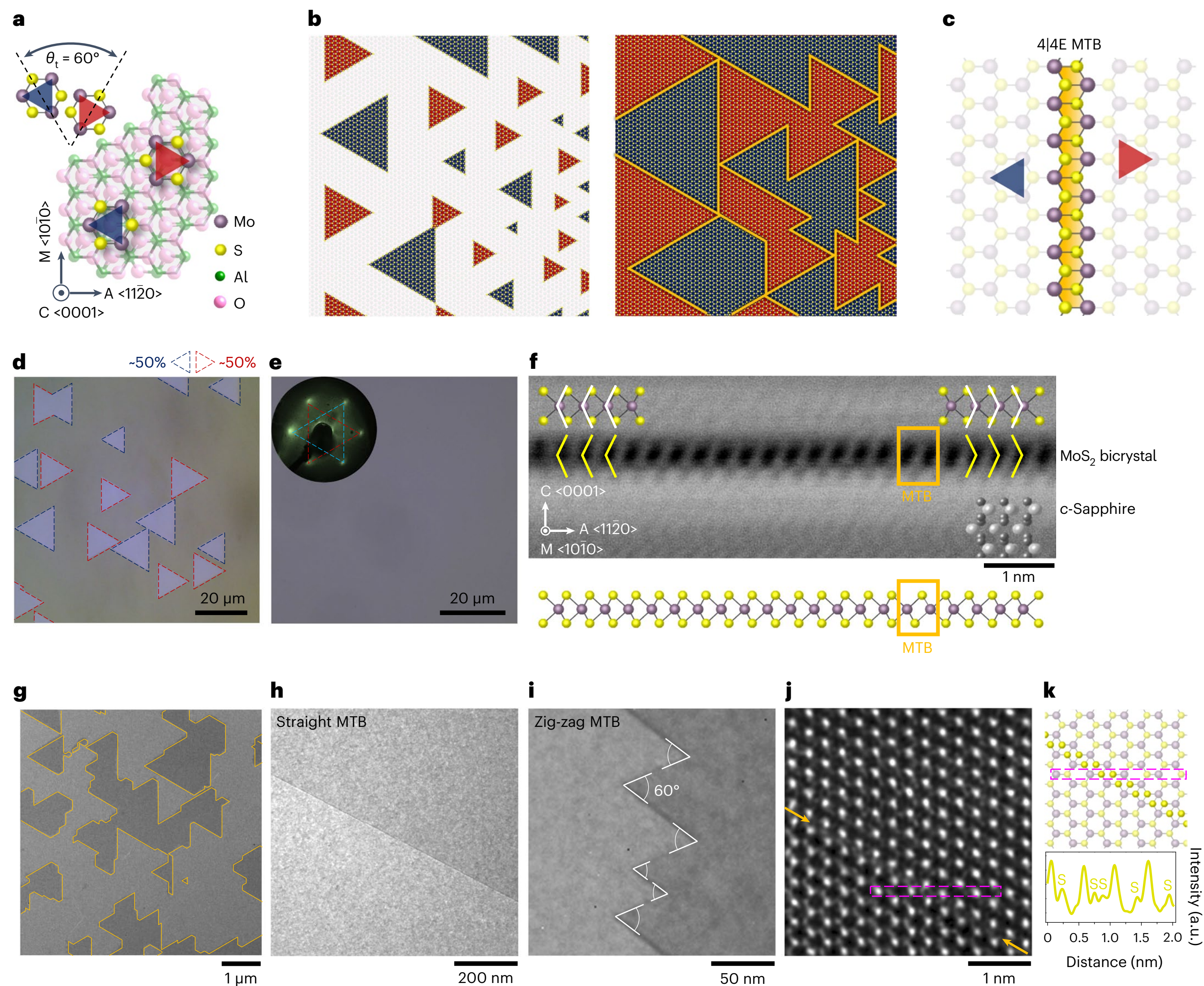

Fig. 1 | MTBs imbedded in epitaxial vdW MoS_2 ML bicrystals. a, Schematics for the two crystallographic variants of threefold MoS_2 ML hexagons on sixfold *c*-plane sapphires by epitaxial relationship. θ_t denotes the tilt angle between the two crystallographic variants. **b**, Schematics for the growth process of MoS_2 ML bicrystal films from two individual crystallographic variants. All grain boundaries (orange lines) are rotated by 60° with respect to each other. **c**, An atomic model for 4|4E MTB in MoS_2 ML bicrystals. **d**, An optical image of homogeneous MoS_2 ML bicrystals grown on a *c*-plane sapphire. Dashed blue and red triangles represent only the two crystallographic variants, for which the number of each crystal facet is statistically 50:50. **e**, An optical image of MoS_2 ML bicrytal films grown on a *c*-plane sapphire. Inset: the representative LEED pattern of MoS_2 ML bicrystals, indicating the sixfold in-plane symmetry by the two threefold variants (dashed blue and red lines). **f**, A cross-sectional BF-STEM image of MTB (orange square) imbedded in MoS_2 ML bicrystals along <10$\bar{1}$0> orientation with the corresponding atomic models. White and yellow lines indicate the bond direction between Mo atoms with their nearest neighbouring S atoms. **g**, An in-plane DF-TEM image of MoS_2 ML bicrystal films stitched by the distinguishable two crystallographic variants at MTBs. The orange lines represent MTBs. **h**,**i**, In-plane DF-TEM images obtained from the straight MTB (**h**) and the zig-zag MTB with 60° kinks (**i**) in MoS_2 ML bicrystals. **j**,**k**, An in-plane HAADF-STEM image (**j**) obtained from the straight MTB segment in MoS_2 ML bicrystals, and the corresponding atomic models (**k**). The orange arrows in **j** indicate the location of the MTB. The line intensity profile in **k** is obtained from the corresponding magenta square in **j**. C, M and A in **a** and **f** indicate the crystallographic axis of *c*-plane sapphires; S, sulfur.

As in Fig. 3c, showing the length-dependent R from 0.5 to 2 μm, we measured the R per unit length of ~0.4 MΩ μm^{-1} in the straight-line MTB channels, which linearly scales with the length, indicating that our MTB lines are ohmic conductors. As shown in Fig. 3d, we have also found that these ohmic characteristics largely persist in diverse junction networks, such as single lines, 60° kinked lines, triangular loops, zig-zag lines and parallel lines (see Supplementary Fig. 17 for the I–V_b characteristics corresponding to each MTB network). Although, in the zig-zag lines, the R values relatively scatter, presumably due to the presence of Mo point defects at the kinks as discussed earlier, their contribution to the total R is negligible; each kink is measured to be an additional series resistor of ~10 kΩ μm^{-1} at 80 K, which is two orders of magnitude smaller than the total R_{MTB}. The parallel MTB lines in Fig. 3d are also measured to be the parallel resistor with the half R_{MTB}.

One-dimensional local gate for ultrascaled transistors

The unique 1D metal networks in our MoS_2 bicrystals can be incorporated to build a new type of vdW device. An obvious feature of these 1D metals is their nominal width of ~0.4 nm to generate local electric field at the atomic scales. We thus integrated the MTB line as a local gate into an FET of single-crystal MoS_2 ML channels, which were separately grown

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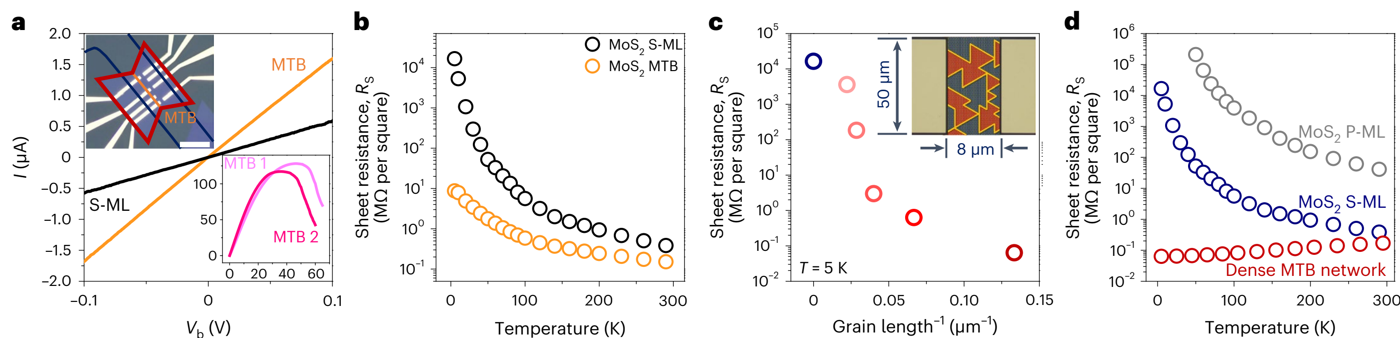

Fig. 2 | 1D epitaxial metal networks in *vdW* MoS_2 ML bicrystals. **a**, Representative I–V_b characteristics of the line MTB channels (orange line) and the MoS_2 S-ML channels (black line), measured at room temperature. Insets: optical image of a MoS_2 ML bicrystal containing both the line MTB channel devices and the MoS_2 S-ML channel devices (top left), and I–V breakdown characteristics of two distinct line MTB channel devices measured at room temperature (bottom right). Scale bar, 10 μm. **b**, Temperature-dependent sheet resistance (R_S) of the MoS_2 S-ML channel (black circles) and the line MTB channel (orange circles). **c**, R_S of the 1D MTB network channels with various grain sizes, measured at 5 K, demonstrating the presence of an electrical percolation threshold. Inset: schematic of a 1D MTB network device with a channel length and width of 8 μm and 50 μm, respectively. **d**, Temperature-dependent R_S of the MoS_2 ML polycrystal (MoS_2 P-ML), MoS_2 S-ML and dense MTB network channels, depicted by grey, blue and red circles, respectively.

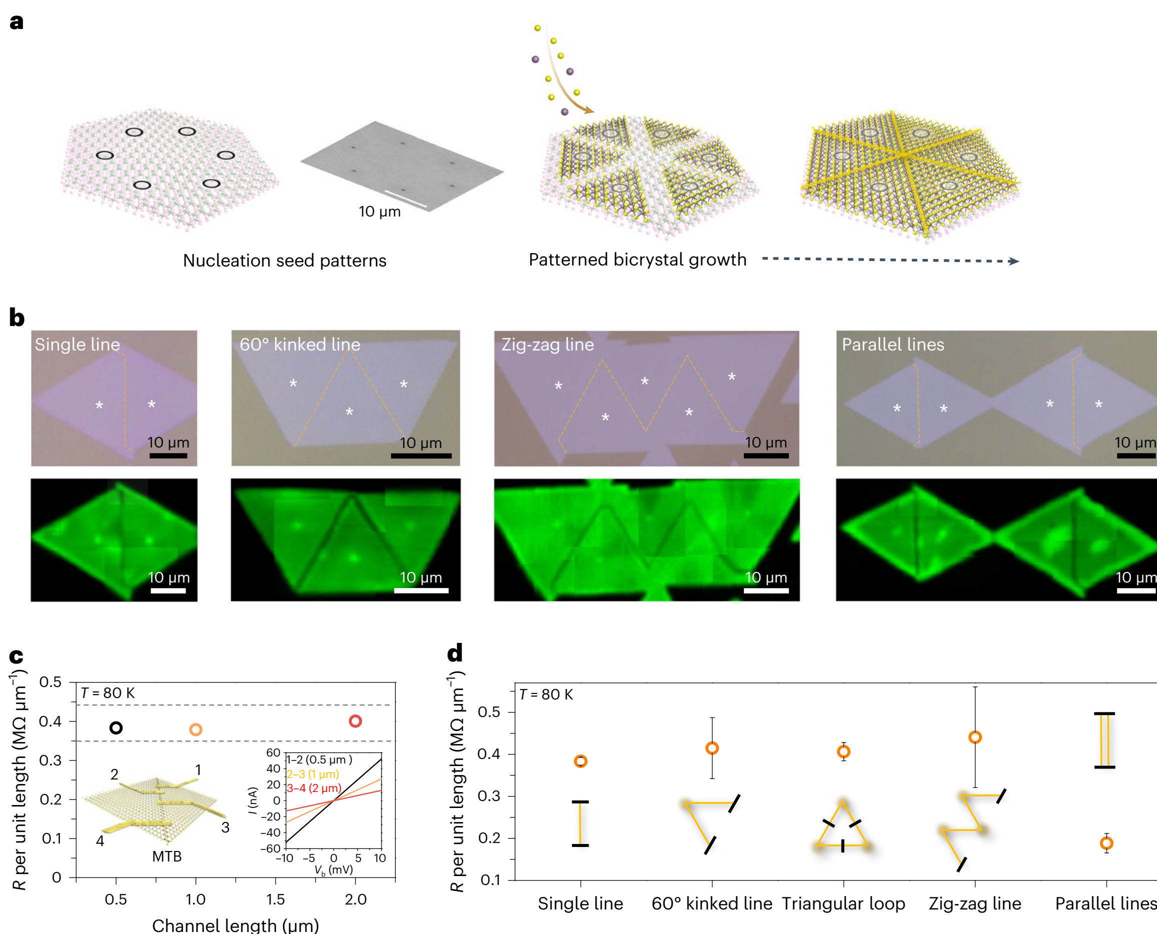

Fig. 3 | Designed 1D epitaxial metal network geometries by position-controlled nucleations. **a**, Schematics of the process for designed MoS_2 ML bicrystals by nucleation seed patterns. Inset: scanning electron microscopy (SEM) image of a *c*-plane sapphire with nucleation seeds patterned in hexagonal shape. **b**, Optical images (top) of designed MoS_2 ML bicrystals with diverse 1D metal network geometries grown on patterned *c*-plane sapphire and SHG mapping images (bottom) corresponding to optical images. The white stars and dashed orange lines depict the nucleation seeds and the expected MTB lines, respectively. Host MoS_2 ML bicrystals and imbedded MTBs are clearly revealed by the reduced SHG intensity at MTBs. **c**, Resistance (R) per unit length of each channel with the corresponding pairs of contacts 1–2 (black circle), 2–3 (orange circle) and 3–4 (red circle) on a straight-line MTB, measured at 80 K. Insets: schematic of the MoS_2 ML bicrystal with four electrical contacts on an imbedded straight line MTB (left), and the corresponding I–V_b curves obtained from each channel (right). The grey horizontal dashed lines illustrate that the resistance per unit length of the straight MTB remains constant regardless of the overall length of the MTB. **d**, R per unit length of the various MTB junction networks, including a single line, a 60° kinked line, a triangular loop, a zig-zag line and parallel lines, measured at 80 K. The error bars represent the standard deviations. Insets: schematics of the devices fabricated on each MTB junction network. Orange lines, black lines and black dots denote the MTB lines, Ti/Au contacts and 60° kinks, respectively.

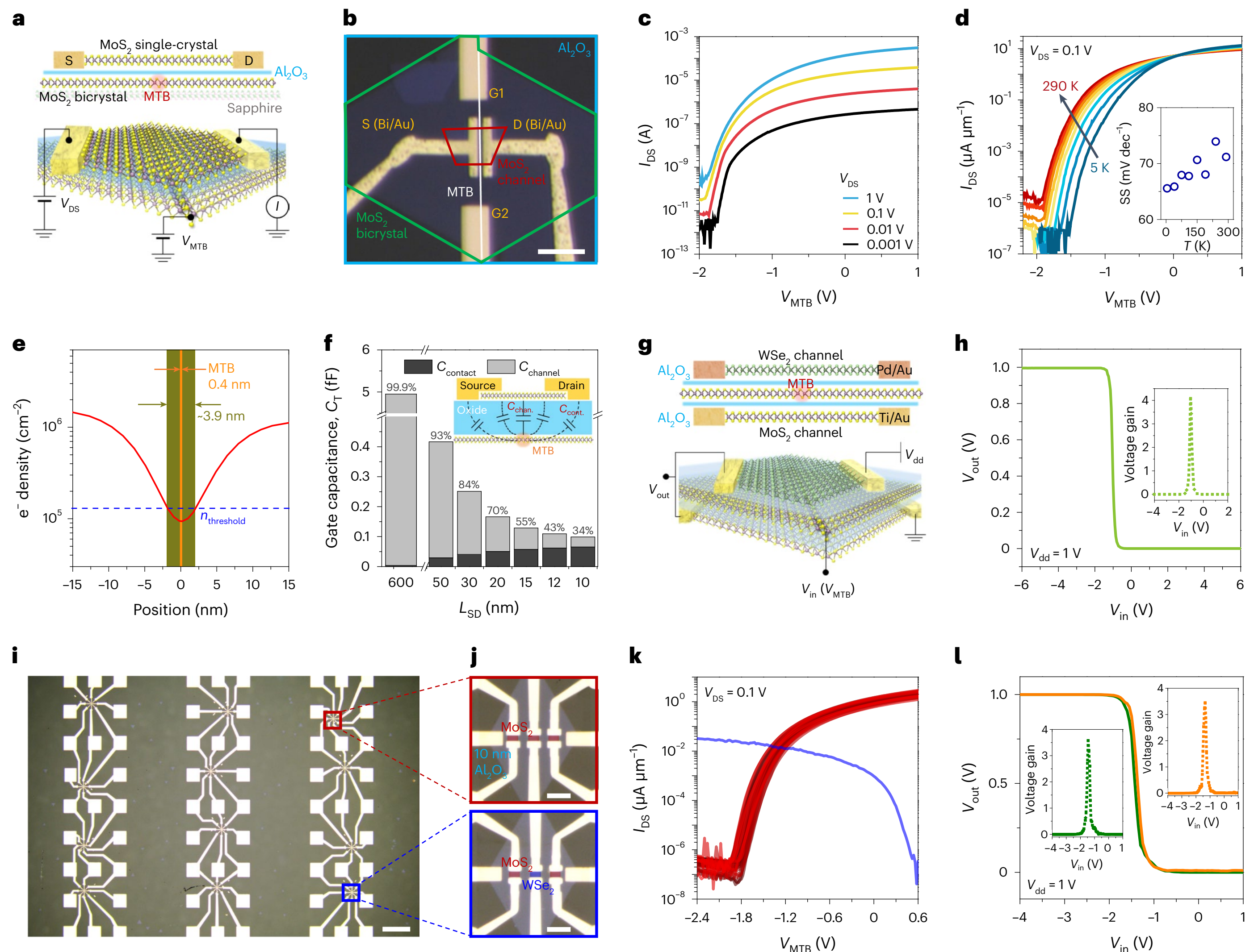

Fig. 4 | FETs with MoS_2 MTBs as 1D local gates. a,b, Schematics (**a**) and an optical image (**b**) of the MoS_2 FET with a 1D MTB gate (G_{MTB}). Scale bar, 5 µm (**b**). **c,d**, Bias voltage (V_{DS})-dependent (**c**) and temperature-dependent (**d**) transfer curves (I_{DS}–V_{MTB}) of the MoS_2 FET with a 1D G_{MTB}. Inset in **d**: SS values at various temperatures from 5 K to 290 K. G1 and G2 represent the gate electrodes that are connected to both ends of the MTB. **e**, Electron density (n) profile near the 1D G_{MTB} and effective depletion channel length (L_{eff}) in $n < n_{threshold}$ ($= 1.3 \times 10^5$ cm^{-2}). The L_{eff} represents the depleted region at $V_{GS} - V_{FB} = 0$ V. **f**, Total gate capacitance (C_T) and its components as a function of the channel length (L_{SD}). The C_T consists of the MTB-to-channel capacitance ($C_{channel}$) and the MTB-to-contact capacitance ($C_{contact}$). Inset: schematic illustrating each capacitance component in our FET device. **g,h**, Schematics (**g**) and voltage transfer characteristics (V_{out}–V_{in}, at $V_{dd} = 1$ V) (**h**) of the CMOS inverter made of the vertical stack of a bottom ML MoS_2 FET and a top ML WSe_2 FET sharing an identical 1D G_{MTB}. Inset in **h**: gain characteristics (dV_{out}/dV_{in}–V_{in}, at $V_{dd} = 1$ V) of the vertical CMOS inverter. **i**, Optical image of a 4 × 3 FET array fabricated on 12 individual straight MTBs. Scale bar, 200 µm. **j**, Enlarged optical images of a unit cell within the red square (top) and the blue square (bottom) in **i**. Each unit cell consists of three FET devices with a channel length and width of 1.3 µm and 1.8 µm, respectively. Red and blue shaded regions represent MoS_2 and WSe_2 ML channels, respectively. Scale bars, 5 µm. **k**, Transfer characteristics of a total of 35 MTB-gated MoS_2 FETs (red curves) and a single WSe_2 FET (blue curve) measured at $V_{DS} = 0.1$ V. **l**, Voltage transfer characteristics of two individual CMOS inverters measured at $V_{dd} = 1$ V, each configured by connecting an n-type MoS_2 FET and a p-type WSe_2 FET built on the common G_{MTB}. Insets: gain characteristics of the two CMOS inverters.

by our vdW vicinal epitaxy[34]. The schematics and the optical microscope image of these FETs are shown in Fig. 4a,b, where a gate stack of a straight MTB and an Al_2O_3 dielectric (5 nm thick by electron-beam evaporation) was placed underneath a single-crystal MoS_2 ML channel (~600 nm long) contacted with bismuth source (S) and drain (D) to achieve an ohmic contact[35]. Notably, we have achieved an on/off switching ratio (I_{on}/I_{off}) of ~10^6 by varying the gate voltage applied to the MTB (V_{MTB}) within the range of −2.2 V to +1 V, as in Fig. 4c,d (see also Supplementary Fig. 18). At a bias voltage (V_{DS}) of 0.1 V, an I_{on} of ~10 µA µm^{-1} was recorded (see Supplementary Figs. 19 and 20 and Supplementary Notes 4 and 5 for the electron mobility of the MoS_2 ML channel in our FET). The subthreshold swing (SS) remains within the range of 65–75 mV dec^{-1} at all temperatures, as in the inset of Fig. 4d (see Supplementary Fig. 21 and Supplementary Note 6 for a comparison with the FET without the 1D MTB gate). These performance metrics are comparable with those of the state-of-the-art MoS_2 FETs towards the ultimate size scaling (see Supplementary Table 1 for detailed comparisons).

The critical role of the 1D MTB gate (G_{MTB}) is to effectively deplete the channel, substantially lowering the I_{off} at lower V_{MTB}, and thus, the atomic-scale gate FET functions were assessed using Synopsys' Sentaurus technology computer-aided design (TCAD) simulation (Methods, Supplementary Fig. 22 and Supplementary Note 7). Figure 4e depicts the electron density (n) variation at the region near the G_{MTB}, when V_{DS} is set to 0.1 V, where the effective depletion channel length is estimated to be ~3.9 nm using a threshold n of ~1.3×10^5 cm^{-2} (ref. 36), which corresponds to ~2.0×10^{12} cm^{-3} in three-dimensional (3D) channels. This implies that

the 1D G_{MTB} modulates the effective n of the <5 nm channels, which satisfies the International Roadmap for Devices and Systems sub-1 nm node target of the channel length (L_{SD}) of ~12 nm (ref. 37). With benchmarks for a dynamic logic circuit application, we simulated the SS and I_{on} characteristics with the L_{SD} scaling down to 10 nm, and found that the SS below ~67 mV dec^{-1} persists until an L_{SD} of ~20 nm (Supplementary Fig. 23a). We have also examined the gate capacitance features arising from the 1D G_{MTB}, as in Fig. 4f. In the extreme scaling Si CMOS technology, the current 3D FETs, such as FinFET and gate-all-around FETs, suffer substantially high parasitic capacitance[37], which arises from the 'global gate'-to-contact fringe capacitance[38]. Here, in our FETs, the spatial extent of the 'local' gate capacitance is extremely narrow and, thus, can be effectively immune to high capacitance, envisaging a new electrostatic scheme towards extreme scaling. The total gate capacitance (C_T), which is a sum of the capacitance between the G_{MTB} and the source–drain contacts ($C_{contact}$) and the capacitance between the G_{MTB} and the MoS_2 channel ($C_{channel}$), substantially decreases with decreasing L_{SD}, benefitting from the small $C_{contact}$. According to the extended circuit simulations (Supplementary Fig. 23b), our MoS_2 ML FETs can scale down to 15 nm from an operation speed perspective and also scale down to 10 nm from a power consumption perspective. Thus, our MoS_2 FETs with the G_{MTB} provide practical implications for the extreme scaling. It should be also noted that the scaling metrics in our FETs can be further improved by optimizing better contacts and effective oxide thickness and so on. As another proof-of-concept device, we demonstrate that our 1D epitaxial gate can be also integrated into a vertical stack of double FETs, where the bottom n-type MoS_2 ML FET and the top p-type WSe_2 ML FET share the common 1D G_{MTB} (Fig. 4g,h; also see Supplementary Fig. 24). These stacks can be configured as a CMOS inverter, where the output voltage (V_{out}) is equal to a supply voltage (V_{dd}) at a negative input voltage ($V_{in} = V_{MTB}$), and V_{out} is zero for a positive V_{in}. The peak DC voltage gain (dV_{out}/dV_{in}) is measured to be up to 4.2 V V^{-1} at $V_{dd} = 1$ V (Fig. 4h, inset).

We extended our 1D epitaxial G_{MTB} device scheme towards integrated circuity by demonstrating the FET arrays. We have grown 12 straight MTBs using our position-controlled growth method and fabricated a 4 × 3 FET array, in which each cell contains three individual FETs sharing a ~20-μm-long single MTB as the common gate (Fig. 4i,j). Each of 11 array cells solely includes three MoS_2 ML FETs (Fig. 4j, top), and the remaining one array cell is composed of two MoS_2 ML FETs and one WSe_2 ML FET to configure the CMOS inverters (Fig. 4j, bottom; also see Supplementary Fig. 25 and Supplementary Note 8). Out of a total of 35 MoS_2 FETs within the array, we have achieved a 100% device yield, with an average SS, I_{on} and I_{on}/I_{off} of 77.1 mV dec^{-1}, ~2.1 μA μm^{-1} and 2.0×10^7, respectively (Fig. 4k). The device-to-device variation, defined as the standard deviation divided by the mean value, of the SS, I_{on}, and I_{on}/I_{off} are 6.0%, 19.6% and 35.4%, respectively. These metrics are comparable to those reported for MoS_2 FET arrays[28,39]. Two individual CMOS inverters exhibit a sharp transition between the two logic states with a similar DC voltage gain of ~3.5 V/V at $V_{dd} = 1$ V (Fig. 4l).

Conclusions

Epitaxial controls over the crystal mosaicity of atomically thin vdW semiconductors in our study, that is, MTBs in MoS_2 ML bicrystals as a local 1D gate, suggest a novel synthetic pathway to construct heterostructure 2D circuitry with scalability. Along with the recent research efforts towards large-area single crystal growth, our observation adds another direction of vdW crystal engineering. Yet, the more precise controls over the crystal textures, such as the uniform size, exact locations and orientation sequence of each crystal facet grain, may further enable the development of innovative 2D electronic circuitries utilizing the metallic MTBs as contacts, interconnects and so on.

Online content

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Methods

Growth of epitaxial MoS_2 ML bicrystals

Epitaxial MoS_2 ML bicrystals were grown on *c*-plane sapphire substrates using our MOCVD system. After loading the sapphire substrate in a hot-walled quartz tube furnace with a diameter of 5 cm, the furnace was ramped up to a growth temperature of 850 °C for 30 min. The total pressure was maintained at 1.7 torr under a carrier gas flow of 90 sccm for Ar (99.9999%) and 4 sccm for H_2 (99.9999%). The growth of MoS_2 ML bicrystals on the sapphire substrate was conducted for 10–90 min. During the growth, $Mo(CO)_6$ and $(C_2H_5)_2S$ were supplied by individual mass flow controllers. The flow rates of precursors were optimized at 0.3 sccm for $Mo(CO)_6$ and 0.6 sccm for $(C_2H_5)_2S$ to grow MoS_2 ML bicrystal films with an average grain size of approximately 25 μm. Nucleation densities were modulated by quantitatively controlling the flow rate of precursors while maintaining the S/Mo ratio using mass flow controllers. By increasing (decreasing) the flow rate of precursors, MoS_2 ML bicrystal films with small (large) grains were induced by high (low) nucleation density (Supplementary Fig. 26). Both precursors were kept in bubbler-type canisters at a constant pressure of 300 torr with Ar, and maintained at room temperature.

Transmission electron microscopy analyses

For the in-plane TEM observations, MoS_2 ML bicrystals were transferred onto Cu TEM grids (holey carbon film grids for dark-field TEM imaging and quantifoil grids for STEM analyses) using polymethylmethacrylate (PMMA)-assisted wet-transfer methods. Specimens for the cross-section TEM observations were prepared by a focused ion beam (Helios NanoLab G3 CX, FEI). For protection, a 20-nm-thick amorphous carbon layer was deposited on top of the specimen using a carbon coater. The imaging in Fig. 1f,j and Supplementary Figs. 1, 7 and 8 was conducted with a JEOL JEM-ARM 200F with a Cs-corrected probe operated at 80 kV. DF-TEM imaging and selected area electron diffraction patterns were performed with a JEOL 2100F with a Cs-corrected probe operated at 200 kV.

Patterning nucleation seeds on *c*-plane sapphire substrate

PMMA was spin coated on the annealed sapphire substrate at 4,000 rpm, and baked at 180 °C. Next, water-soluble charge conducting polymer (a mixture of Triton X-100 and PEDOT:PSS (1.3 wt.%) with a mass ratio of 1:99) was spin coated over the PMMA. Then, nucleation seeds with a diameter of 500 nm were patterned by electron-beam lithography. After the removal of the conducting polymer using deionized water and the development of nucleation seeds using a mixture of methyl isobutyl ketone and isopropyl alcohol (in a 1:3 ratio), our Ar ion milling system was carried out at 0.41 kV for 1 min. The residual PMMA mask layer was removed by acetone.

Device fabrication on insulating *c*-plane sapphire substrates

Devices fabricated on epitaxial MoS_2 ML bicrystals on *c*-plane sapphire substrates were made by using electron-beam lithography and electron-beam evaporation for electrodes (Ti 10 nm/Au 40 nm). As the *c*-plane sapphire substrates are electrically insulating, we applied a water-soluble charge conducting polymer to mitigate the charging effect during the electron-beam lithography process. Specifically, we used a mixture of Triton X-100 and PEDOT:PSS (1.3 wt.%) with a mass ratio of 1:99, which was spin coated over the e-beam resist PMMA layers. To fabricate the MoS_2 FET with a 1D G_{MTB}, we initiated the process by depositing a 5 nm layer of Al_2O_3 onto a MoS_2 ML bicrystal using electron-beam evaporation. Following this, we employed PMMA-supported wet-transfer methods to transfer an epitaxial MoS_2 ML single-crystal onto the bicrystal, which had previously been coated with Al_2O_3. Subsequently, Bi/Au (15 nm/35 nm) contact electrodes were integrated into the MoS_2 ML single-crystal channel, completing the FET fabrication. To create the vertical stack of double FETs, we initially picked up and transferred an epitaxial MoS_2 ML single-crystal onto a SiO_2 (100 nm)/p^+-Si substrate. We then fabricated Ti/Au (2 nm/10 nm) contact electrodes on the MoS_2 ML single crystal and deposited the first Al_2O_3 layer (15 nm) on top. Subsequently, we positioned an epitaxial MoS_2 ML bicrystal onto the first Al_2O_3 layer, ensuring that the imbedded MTB spatially overlapped with the MoS_2 ML single-crystal channel. Following this alignment, we created Ti/Au (5 nm/15 nm) electrodes on both ends of the MTB and added a second Al_2O_3 layer (15 nm) on top. Lastly, we transferred an exfoliated ML single-crystal of WSe_2 onto the second Al_2O_3 layer and fabricated Pd/Au (15 nm/20 nm) electrodes on it.

Electron transport measurements

We conducted room temperature transport measurements using a cryogenic probe station (PS-100, Lake Shore Cryotronics) under vacuum conditions (pressure less than 10^{-5} torr). For temperature-dependent electrical measurements down to 5 K, we utilized a helium vapour flow cryostat (CryoAdvance 50, Montana Instruments). All measurements were carried out using a semiconductor parameter analyser (Keithley 4200, Tektronix).

C-AFM

We conducted C-AFM experiments using scanning probe microscopy equipment (Bruker, MultiMode-V with Nanoscope controller V and TUNA module) in ambient conditions at room temperature. To perform these experiments, we employed a conductive diamond-coated AFM probe (NANOSENSORS, CDT-FMR-10). We captured the current map using a scan rate of approximately 20 μm s^{-1} with a resolution of 512 lines or points. The C-AFM equipment was set to a current sensitivity of 100 nA V^{-1}, and the typical noise level observed during measurements was approximately 100 pA.

SHG measurements

SHG signals were measured under ambient condition by using a femtosecond Ti:sapphire laser, at a central wavelength of 800 nm with a pulse repetition rate of 80 MHz. An objective lens of a numerical aperture 0.6 was used to focus the laser beam to a spot size of approximately 1 μm and to collect SHG signals in the back-scattering geometry. For the spatial mapping of the SHG signals, we used a piezo-actuated stage.

TCAD simulations

We conducted the electrical analysis of the device using Synopsys Sentaurus, a 3D TCAD software package from Synopsys. To develop an ML MoS2 library as the channel material, we utilized density functional theory simulation results[40,41]. Additionally, information on the in-plane and out-of-plane dielectric constants of the vdW material was also used[42]. For the analysis of electrical transport characteristics, we employed a drift–diffusion model, which incorporates a high-field saturation model and a thin layer model. It is worth noting that we used the Enormal model to describe phonon, Coulomb and surface roughness scattering near the channel–oxide interface. Furthermore, we used Bi as the contact metal for MoS_2, which resulted in an ohmic contact, a well-established outcome in prior research[35]. This choice enabled us to set the Schottky barrier height to 0 eV.

Data availability

Presented measurement data within this article and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

H.A., G.M. and M.-H.J. conceived and designed the project. H.A., H.C. and C.-J.K. conducted the MOCVD growth experiments and material characterizations. G.M., B.D., C.H. and H.P. fabricated the devices and performed the electrical measurements. S.Y. and J.K. conducted the SHG measurements. H.J., J.J. and J.-H.P. carried out the TCAD simulations. D.-H.Y. and S.-Y.C. performed the TEM measurements and analysed the data. Y.Y. and C.-H.Y. performed the C-AFM measurements. H.A., G.M. and M.-H.J. wrote the paper. M.-H.J. supervised the project. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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