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Pristine Graphene Insertion at the Metal/Semiconductor Interface to Minimize Metal-Induced Gap States

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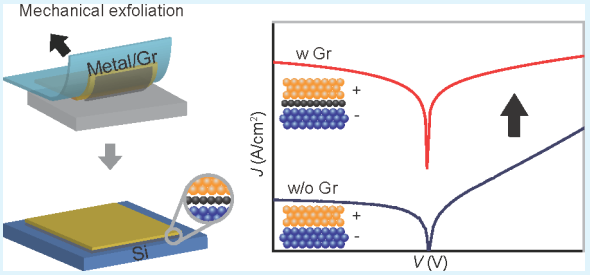
ABSTRACT: Metal (M) contact with a semiconductor (S) introduces metal-induced gap states (MIGS), which makes it difficult to study the intrinsic electrical properties of S. A bilayer of metal with graphene (Gr), *i.e.*, a M/Gr bilayer, may form a contact with S to minimize MIGS. However, it has been challenging to realize the pristine M/Gr/S junctions without interfacial contaminants, which result in additional interfacial states. Here, we successfully demonstrate the atomically clean M/Gr/*n*-type silicon (Si) junctions via all-dry transfer of M/Gr bilayers onto Si. The fabricated M/Gr/Si junctions significantly increase the current density J at reverse bias, compared to those of M/Si junctions without a Gr interlayer (e.g., by 10^5 times for M = Au in Si(111)). The increase of the reverse J by a Gr interlayer is more prominent in Si(111) than in Si(100), whereas in M/Si junctions, J is independent of the type of Si surface. The different transport data between M/Gr/Si(111) and M/Gr/Si(100) are consistent with Fermi-level pinning by different surface states of Si(111) and Si(100). Our findings suggest the effective way to suppress MIGS by an introduction of the clean Gr interlayer, which paves the way to study intrinsic electrical properties of various materials.



KEYWORDS: *metal contact, Schottky barrier, metal-induced gap states, graphene interlayer, dry transfer*

INTRODUCTION

Metal/semiconductor (M/S) junctions have important functions in electronics. The electron current flow between M/S junctions depends on an electronic energy barrier, known as the Schottky barrier $e\Phi_B$.[1] If intimate contact with abrupt and lack of additional states is assumed at M/S interfaces, then according to the Schottky–Mott model, $e\Phi_B$ is determined by the bulk properties of M/S, and the $e\Phi_B$ for electron becomes equivalent to the difference between metal work function W_M and the semiconductor electron affinity. In reality, M/S interfacial states strongly affect the barrier properties, so $e\Phi_B$ depends weakly on W_M by Fermi-level pinning. Deposition of metals onto semiconductor surfaces can form a metal-induced gap state (MIGS) within the band gap of the semiconductor.[2] As a result, the MIGS determines the Fermi-level pinning point and the $e\Phi_B$ and thereby affects the current flow across the junction. Intentionally introduced thin interlayers including ZnO and TiO_2 can suppress the formation of MIGS by reducing M/S interactions and effectively modulate $e\Phi_B$.[3−5] However, current decays exponentially as the thickness of the barrier increases, and fabrication of an interlayer that has a thickness of a few nanometers and has uniform thickness at the atomic scale is a difficult task. Also, the deposition process can change the intrinsic surface structures, so control of the interfacial states may be difficult.

Two-dimensional (2D) materials that are free-standing with a thickness of only a few atoms and that have self-passivated surfaces can be an ideal barrier to minimize MIGS on M/S interfaces. These materials can form contacts with semiconductors without forming a direct chemical bond, so they do not affect the pristine surface structure of semiconductors, as well as provide a uniform subnanometer thickness. Among various 2D materials, graphene (Gr) has several ideal characteristics for use as an interlayer: its one-atom thickness can maximize tunneling current; its high chemical and thermal stability prevents possible damage to the film during metallization; and a semimetal characteristic with linear band dispersion can be fully metallized by interfacing with various metal species to modulate the work function over a broad energy range.[6]

Previous studies on electrical transport across M/Gr/silicon (Si) junctions have shown several distinct properties, compared to M/Si junctions without Gr. These include modulation of W_M and $e\Phi_B$ with low contact resistance,[7] high tunneling current,[8] and reduced leakage current.[9,10] However, independent studies on similar M/Gr/Si junctions show largely different properties, so the exact function of a Gr

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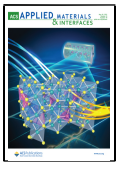

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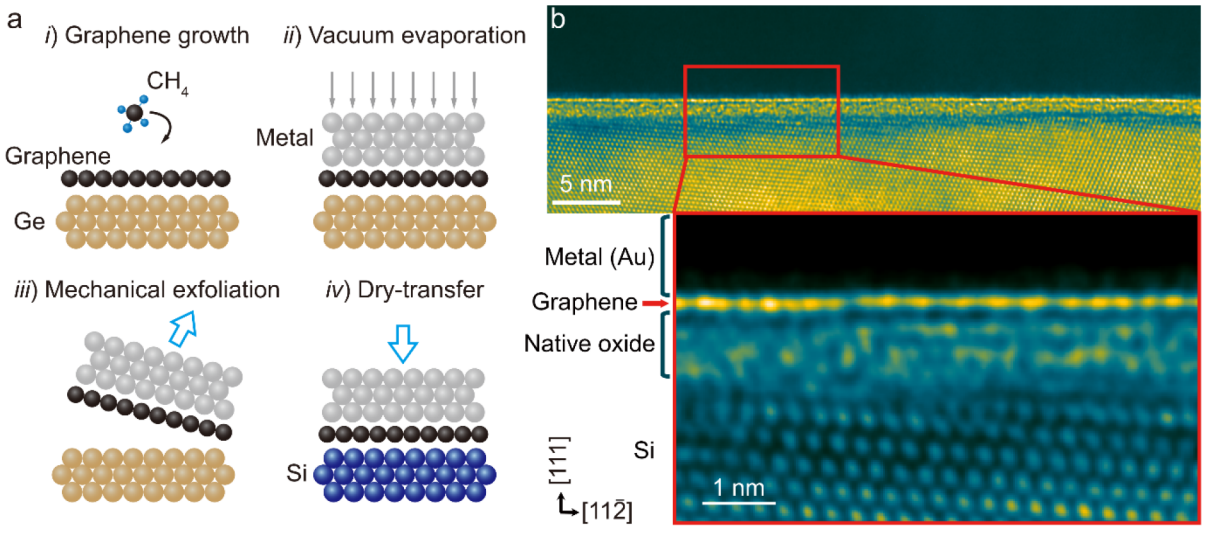

Figure 1. (a) Schematics of fabrication steps for M/Gr/Si junctions. (i) Growth of Gr films on Ge(110) surfaces by CVD of CH_4. (ii) Deposition of metal superlayers on Gr by thermal evaporation in vacuum. (iii) Mechanical exfoliation of M/Gr bilayers from Ge(110). (iv) Transfer of M/Gr bilayers onto Si surfaces. (b) Cross-sectional bright field HRTEM image of Au/Gr/Si(111) junction. The upper image is the low magnification of the Au/Gr/Si cross-section. The zone axis of Si is set to [110] direction. The bright linear contrast crossing the center horizontally is the Gr cross-section and is indicated by red arrow. Scale bar: 5 nm. The lower image is the high magnification of upper data which is marked with a red square. Since the Gr zigzag edge is aligned with Si (110), the C atoms form a column. Deposited Au is on the Gr, and below the Gr is 1 nm thickness-native oxide and Si, respectively. Scale bar: 1 nm.

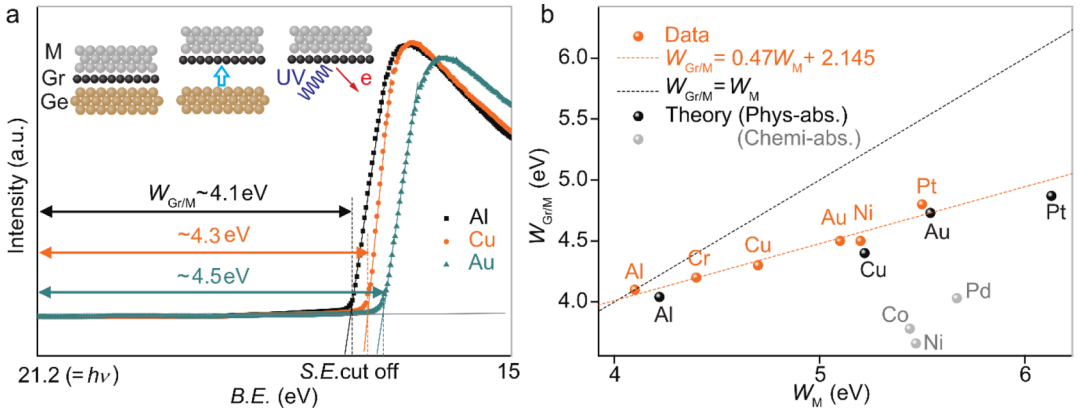

Figure 2. (a) Inset: Schematics of UPS experiments on exfoliated M/Gr surfaces. Main: Intensity of photoelectrons as a function of binding energy (B.E.), which is the energy difference between the incident photon and the emitted photoelectron. (b) $W_{Gr/M}$ as a function of W_M for experimental data (orange spheres; orange broken line) and theoretical calculations from reference (black spheres: physisorbed Gr, gray spheres: chemisorbed Gr; black broken line: $W_{Gr/M} = W_M$). Reprinted with permission from ref 6. Copyright 2008 American Physical Society.

interlayer remains unclear. For instance, the same M/Gr contacts on *n*-type Si have shown Fermi-level pinning at different energy levels from near the conduction band minimum to near the valence band maximum.[7,9]

Contaminants in the M/Gr/Si junctions during fabrication is a plausible reason for the inconsistent $e\Phi_B$. Even a small quantity of impurities can induce additional interfacial states that change the doping level of an atomically thin interlayer; therefore, to obtain the designed properties, M/Gr/Si junctions must be formed with the atomically clean interfaces. One way to form pristine junctions is by direct growth of Gr on semiconductors of interest in vacuum environment; however, the method is currently limited to a few semiconductors, such as Ge and SiC.[11,12] As an alternative method, Gr can be transferred onto arbitrary semiconductors including Si to verify the effect of the Gr interlayer on the electrical properties of various M/S junctions. However, the transfer process typically involves wet-etching processes, which unavoidably leave ionic, polymer, and metal impurities at the final interfaces,[13] so the intrinsic properties of clean M/Gr/Si interfaces remain elusive.

Here, we demonstrate fabrication of pristine M/Gr/Si junctions on lightly *n*-type doped Si ($N_d = 10^{15}$ cm^{-3}) without exposing Gr interfaces to other wet chemicals. In comparison with M/Si junctions without a Gr interlayer, metallized Gr/*n*-Si junctions for various metals showed significantly different electrical characteristics; this result indicates effective suppression of MIGS.

RESULTS AND DISCUSSION

To form atomically clean interfaces at M/Gr/Si junctions, we used an all-dry transfer method (Experimental Section; Figure S1), by which Gr film can be transferred onto arbitrary substrates without use of any wet chemicals. The processes consist of four steps (Figure 1a). (i) Gr films were grown on

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polished Ge(110) surface by chemical vapor deposition (CVD) using CH_4 precursor. The high quality and uniformity of Gr films were confirmed by Raman spectroscopy (Figure S2). (ii) On the Gr surface, a thermally evaporated metal superlayer was deposited in vacuum to form M/Gr junctions. (iii) The M/Gr bilayers were mechanically exfoliated from the Ge(110).[11,14] (iv) Exfoliated M/Gr bilayers were transferred onto Si surfaces.

The Au/Gr/*n*-type Si(111) junction was cross-sectionally imaged by high-resolution transmission electron microscope (HRTEM) shown in Figure 1b and scanning transmission electron microscopy (STEM) shown in Figure S3a. The Au and *n*-type Si were clearly separated by a single Gr layer, a bright line across the interface, which implies that Au did not damage the Gr layer during the evaporation (step ii),[15] nor did the Au diffuse into the Si to form an alloy after the transfer process (step iv). Prevention of metal diffusion into Si by the Gr interlayer was further confirmed by the lack of metal-induced scattering signals in annular bright-field scanning transmission electron microscopy (ABF-STEM) (Figure S3a). The Gr interfaces also showed no indications of hydrocarbon bubbles, which are often introduced in Gr samples that are transferred by wet-transfer methods.[13] The Au layer directly contacted the Gr layer (Figure S3b), and only a native oxide layer with thickness ~1 nm existed between the Gr and Si.

This all-dry transfer process enables systematic study of the true electrical properties of Gr heterointerfaces. The work functions $W_{Gr/M}$ of metallized Gr layers with different metals were investigated before they were used to form junctions with semiconductors. Ultraviolet photoelectron spectroscopy (UPS) experiments on pristine metallized Gr surfaces were conducted immediately after the exfoliation from Ge to avoid air-borne contaminants, and $W_{Gr/M}$ was deduced from the difference between incident photon energy and secondary electron cutoff energy (Figure 2a).

To quantify the difference between $W_{Gr/M}$ and the work functions W_M of pure metal, the measured $W_{Gr/M}$ were plotted as a function of W_M (Figure 2b, orange broken line), which follows the relationship $W_{Gr/M} = 0.47W_M + 2.145$. The clear deviation from $W_{Gr/M} = W_M$ (black broken line) indicates significant modulation ΔW (= $W_M - W_{Gr/M}$) of W_M by Gr film with charge transfer between Gr and M. The slope $dW_{Gr/M}/dW_M < 1$, and $\Delta W = 0$ at $W_M = 4$ eV. First-principles calculations by density functional theory (black spheres) on the relationship between $W_{Gr/M}$ and W_M predict similar $dW_{Gr/M}/dW_M \sim 0.5$ and $\Delta W = 0$ when $W_M = 4$ eV for Gr on metal with physisorption.[6] The theory overestimates the work function values for given M, compared to the experimental data, but ΔW for a specific W_M may still be correct, as the charge transfer between Gr and M to determine ΔW is mainly set by the absolute W_M value rather than the type of M. Naively, one would expect that ΔW becomes 0 with zero charge transfer when W_M equals the work function W_{Gr} of isolated Gr, which is experimentally measured as roughly 4.6 eV. However, the interfacial dipoles between M and Gr can change the offset value for zero-charge transfer to 4 eV.[6] The theory also predicts that chemisorption occurs between Gr and strongly interacting metals such as Co, Ni and Pd and significantly reduces $W_{Gr/M}$ (gray spheres) by significantly enhanced charge transfer. However, the measured $W_{Gr/M}$ for the M in this study shows much smaller ΔW; this observation indicates that in this case, in which evaporated metal was deposited on Gr, chemisorption did not happen, possibly because interlayer interactions were limited by the large lattice mismatch (e.g., 1.3% between Gr and Ni(111)).[16] Several experimental studies of $W_{Gr/M}$ have been reported,[7,17,18] but our data are the first confirmation of the theory by demonstrating linear modulation of $W_{Gr/M}$ by W_M, and zero charge transfer at $W_M = 4$ eV. The data (Figure 2) collectively suggest that $W_{Gr/M}$ with different metals form pristine interfaces; this variation may enable control of $W_{Gr/M}$ values over a broad energy range.

Now, we study the electrical properties of M/Gr/Si junctions. A series of M/Gr/Si junctions that used different metals were fabricated by all-dry transfer of metallized Gr with controllable $W_{Gr/M}$ onto Si surfaces. Lightly *n*-type-doped (10^{15} cm^{-3} by phosphorus dopants) Si(111) and Si(100) surfaces were treated with oxide etchants before the transfer of M/Gr bilayer onto them. The all-dry transfer is critical to observe reproducible electrical properties because the exposure of Gr surfaces to wet chemicals dramatically changes the electrical current across the M/Gr/Si junctions (Figure S4). Spatial uniformity of the M/Gr/Si junctions was verified by measuring electrical properties in a batch-fabricated array of junction devices over an area of a few square millimeters (Experimental Section and Figure S5). Data in the main text were collected from single-junction devices. Current density *J*-voltage *V* characteristics (Figure 3) were measured at room

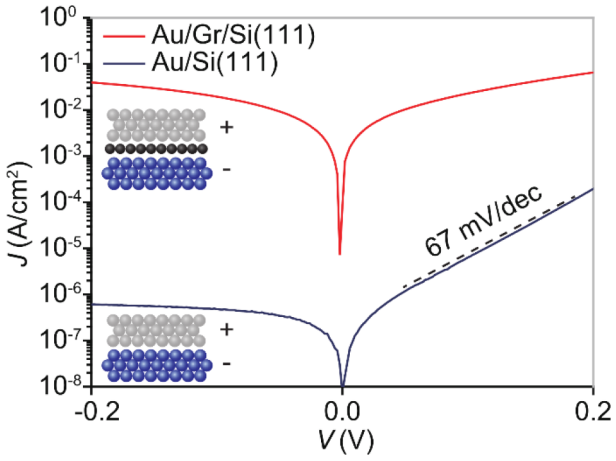

Figure 3. *J*–*V* characteristics for Au/Gr/Si(111) (red curve) and Au/Si(111) junctions (blue). Inset: Schematics for the junctions with the indication of the applied bias polarity.

temperature (rt) across Au/Gr/Si(111) and Au/Si(111) junctions, then compared to verify the effect of Gr interlayer on the electrical properties. The Au/Si(111) junction showed typical rectifying behavior of a Schottky diode with the expected bias polarity for Au and *n*-type Si. *J* saturated during reverse bias, and threshold swing in the forward bias region was 67 mV/dec, which is close to the ideal value of 60 mV/dec in thermionic emission (TE) theory.[1] Strikingly, in contrast, the Au/Gr/Si(111) junction showed a significantly more symmetric curve and ~10^5 times higher reverse bias *J*, compared to the Au/Si(111) junction without the Gr interlayer. Previous studies on similar M/Gr/Si systems show only 1–10 times change of the reverse bias *J* at rt, compared to M/Si.[7,9,10]

To further understand the exact function of the Gr interlayer, the electrical properties of M/Si and M/Gr/Si junctions were further compared by metallic types (Al, Cr, Cu,

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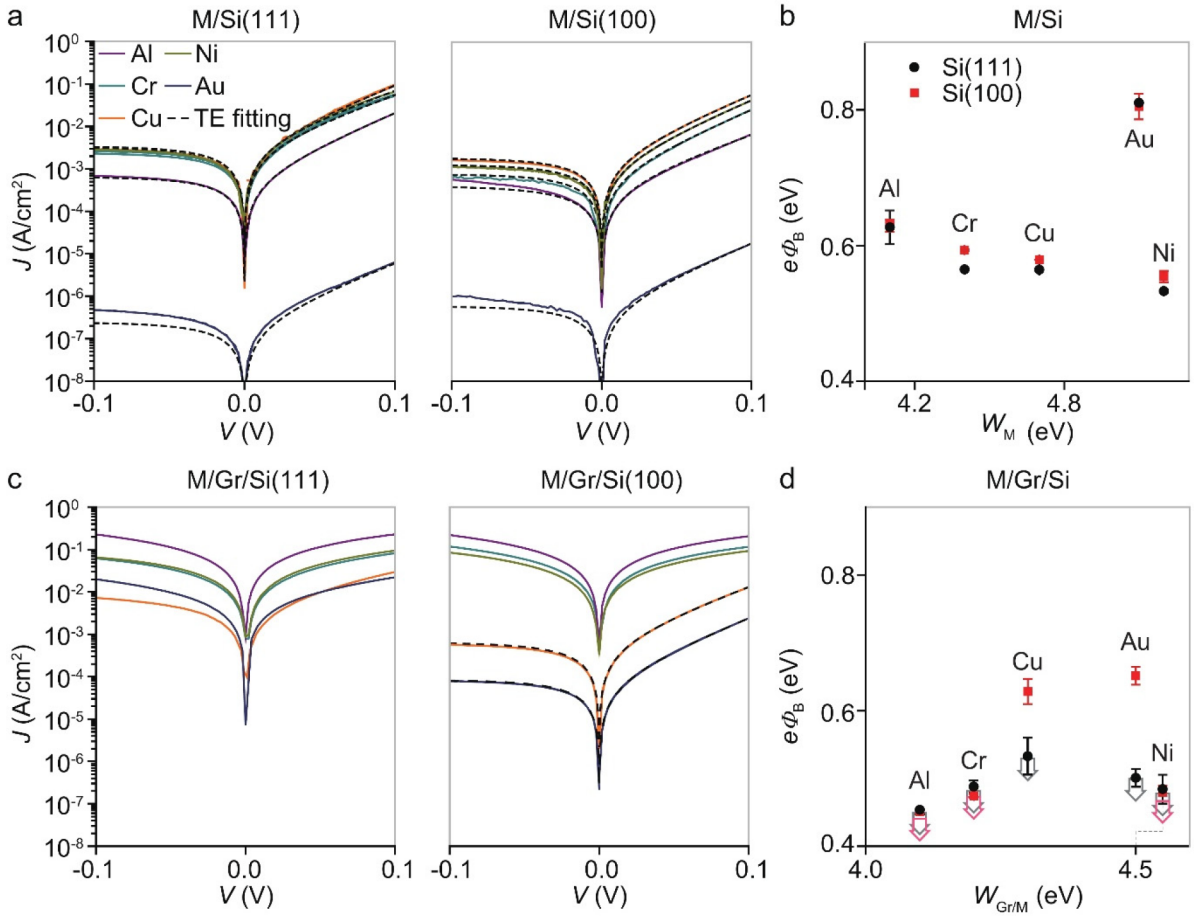

Figure 4. (a,c) J–V characteristics of (a) M/Si(111) and M/Si(100) and (c) M/Gr/Si(111) and M/Gr/Si(100) junctions with different M. (b,d) Experimentally deduced $e\Phi_B$ as a function of work functions for (b) M/Si and (d) M/Gr/Si with different M (from left to right: Al, Cr, Cu, Ni, and Au) and Si surface conditions (black spheres: Si(111), red squares: Si(100)). In M/Gr/Si, data for Ni are shifted to the right for clarity, which have the same $W_{Gr/M}$ as Au. Error bars: ± 1 s.d., $n \geq 3$. Arrows mean that actual $e\Phi_B$ is lower than the presented values.

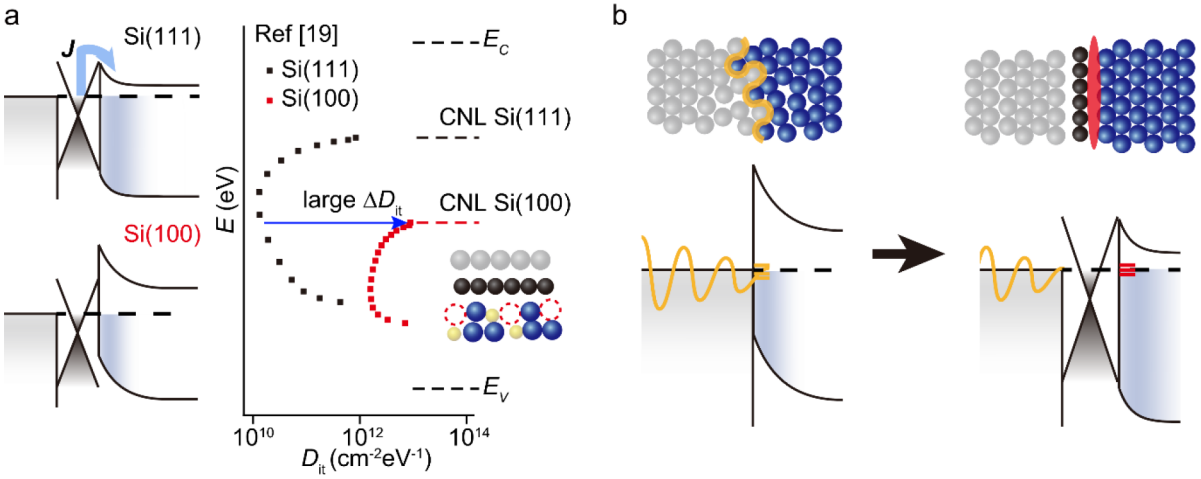

Figure 5. (a) (Left) Schematics for electronic band profiles across M/G/Si junctions with different Si surfaces. (Right) D_{it} distribution within the band gap of Si for Si(111) and Si(100) surfaces. Reprinted with permission from ref 19. Copyright 2000 Elsevier. Inset: Schematic for the atomic structure at M/Gr/Si junctions with vacancies (red dotted circles). (b) Proposed models for atomic structures and electronic band profiles for M/Si (left) and M/Gr/Si junctions (right). Yellow wave: extended electronic states from metals; yellow lines: extended electronic states of MIGS; red lines: surface states of Si.

Ni, and Au) and/or the surface orientations (Si(111) and Si(100)). All of the measured J–V characteristics on M/Si junctions for various metals and Si surfaces (Figure 4a) showed typical rectifying behaviors, following the TE model for Schottky junction with ideal factors η < 1.5 (Experimental Section and Table S1). The deduced $e\Phi_B$ for different metals

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from several samples (Figure 4b) were similar to previous reports on M/Si junctions.[7] The change of M from Au to Al with lower W_M than Au accordingly yielded a significant reduction in $e\Phi_B$ by ~0.2 eV. However, $e\Phi_B$ is invariable to the Si surface orientation.

In contrast, introduction of a Gr interlayer results in a substantial difference between the electrical properties of M/Gr/Si(111) and M/Gr/Si(100) junctions (Figure 4c). In M/Gr/Si(111) junctions, the $J-V$ curve was symmetrical for all the metals with increased reverse bias J; this response does not conform to the TE model. On the other hand, M/Gr/Si(100) junctions show rectifying $J-V$ characteristics, which are consistent with thermionic currents of $\eta < 1.5$ (Table S1) for M = Cu and Au, and the $J-V$ curve of M/Gr/Si(100) junctions for M = Al, Cr, and Au is similar to one from M/Gr/Si(111). We deduced $e\Phi_B$ from both rectifying and nonrectifying $J-V$ data. The rectifying $J-V$ data were fitted by the TE model (broken line in Figure 4c) to estimate $e\Phi_B$ (Table S1). Nonrectifying $J-V$ characteristics are typically observed when the series resistance is higher than the contact resistance from the Schottky junction, so the upper limits of $e\Phi_B$ can be deduced (Figure S6) by considering the measured resistance to be a Schottky-junction resistance. The Gr interlayer substantially lowered $e\Phi_B$ for both M/Gr/Si(111) and M/Gr/Si(100) with $W_{Gr/M} < W_M$, as measured in Figure 2. However, the $e\Phi_B$ was lower in M/Gr/Si(111) than in M/Gr/Si(100), especially for M = Cu and Au, even though they had the same $W_{Gr/M}$.

Now, we discuss why the electrical properties of metallized contacts on Si strongly depend on the Si surface structures only when the Gr interlayer is present for M = Cu and Au. Measured electrical characteristics on each Si surface were used to guide development of schematic electronic structures for M/Gr/Si junctions that had different junction barriers for each Si surface (Figure 5a). In the Fermi-level pinning model,[1] a Fermi level forms near the charge-neutrality level (CNL), which is an interface state in which coincidence with Fermi-level makes zero net trap charge and, therefore, determines $e\Phi_B$. The difference between $e\Phi_B$ of M/Gr/Si(111) and $e\Phi_B$ of M/Gr/Si(100) indicates that the different Si surface conditions make an important contribution to the distribution of interface states in the energy level, only in the case of the soft metallization by transfer of M/Gr layer on Si. Indeed, the energy level of intrinsic Si(111) and Si(100) surface states, deduced by surface photovoltage measurements[19,20] are consistent with the Fermi-level positions, corresponding to the measured $e\Phi_B$ in M/Gr/Si junctions (Figure 5a). According to an electronegativity model with a consideration of Fermi-level pinning, $e\Phi_B$ depends on the Si surface potential, as well as the energy difference between Si and metal potentials.[2] When the Fermi level of metal is located between the different CNL levels of Si(111) and Si(100), charge transfer can occur in opposite directions, reducing the $e\Phi_B$ difference between two Si surfaces. This is the case for low $W_{M/Gr}$ with Al and Cr, which indeed shows a weak surface dependency in $e\Phi_B$ (Figure 4d).

The density distribution D_{it} of surface states in Si(111) shows a broad U-shape within the band gap, with high D_{it} near band edges as a result of strained Si−Si bonds at the interfaces and low D_{it} in the middle of the band gap. In contrast, in Si(100) surfaces, D_{it} in the middle of the band gap substantially increases (blue arrow in Figure 5a), so the total distribution of D_{it} shifted toward the middle of the band gap. The states are believed to be associated with dangling bonds, which are abundant within native oxides on Si (right inset in Figure 5a). In particular, the native oxide layer on Si(100) surfaces tends to be more porous with a higher density of dangling bonds than the oxide on Si(111) because of the different atomic configuration and high roughness of the Si(100) surfaces.[19] We observed a substantially thicker oxide layer (about 2 nm) in the cross-sectional TEM image on Au/Gr/Si(100) devices (Figure S7), compared to Au/Gr/Si(111) (Figure 1b). If the CNL forms at the energy level that has the highest D_{it}, then the $e\Phi_B$ will be ~0.6 eV for Si(100) and <0.3 eV for Si(111); these expectations are consistent with our experimental results.

Conventional metallization onto Si surfaces by evaporated metal can alter the interfacial states (orange colored states in Figure 5b) by resulting in development of substantial MIGS with metallurgical reaction, formation of direct M/Si bonds, and extension of electronic states from metal into Si.[21,22] Thus, the drastic changes of $e\Phi_B$ in M/Gr/Si junctions, and strong dependence on Si surface states, suggest that the dangling bond-free Gr interlayer effectively eliminates MIGS by screening interatomic mixing/bonding and penetration of electronic states (Figure 5b) without forming chemical bonds with the Si surfaces. X-ray photoemission spectroscopy (XPS) data (Figure S8) showed that the Gr interlayer indeed suppressed the metallurgical reactions at M/Si interfaces without reacting with the Si surfaces.[23]

The $e\Phi_B$ can be controlled to a degree by changing W_M, especially with the Gr interlayer. The insertion of the Gr interlayer reduces the $e\Phi_B$ of M/S junctions for all the tested metals. In general, $W_{M/Gr}$ is lower than W_M, resulting in the effective reduction of $e\Phi_B$ with Fermi-level depining phenomena. We note that Ni in both M/Si and M/Gr/Si junctions shows exceptionally low $e\Phi_B$ even with the high W. This observation is consistent with previous studies on Ni/Si junctions[1] and Ni/Gr/Si junctions with clean interfaces,[24] which ascribe the low $e\Phi_B$ to the strong interactions between Ni and Si by low electronegativity of Ni.[25,26] Therefore, we deduced the slope of $de\Phi_B/dW$ for M/Gr/Si and M/Si junctions, precluding the case of Ni. The $de\Phi_B/dW$ is higher in M/Gr/Si(100) as ~0.55 than ~0.3 in M/Si(100), indicating that the Gr interlayer not only causes the CNL level to be set by intrinsic Si surface states but also reduces D_{it} by minimizing MIGS. Therefore, electrical contacts with metallized Gr can be useful to study the intrinsic properties of semiconductors that have fragile surfaces, such as metal halide perovskites, organic materials, and topological semimetals.[27−29]

CONCLUSIONS

Significant modulation of $e\Phi_B$ was achieved in the metallized contacts on lightly doped n-type Si by introducing an atomically clean Gr interlayer at M/Si interfaces. The surface state of Si has an important influence on $e\Phi_B$ in M/Gr/Si interfaces, but not at M/Si interfaces. We conclude that development of MIGS was minimized by Gr insertion with pristine interfaces, which leave the surface intact. Our results provide a new insight on the function of the Gr interlayer in a Schottky junction and provide a versatile method to precisely engineer the interaction between two materials. The approach can be further useful in various applications, in which formation of pristine interfaces with atomically thin interlayers is critical to obtain the desired junction properties; examples include Josephson junctions,[28] optical excitation states at semiconductor heterojunctions,[29,30] and remote epitaxy for growth of transferrable crystalline materials.[31]

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EXPERIMENTAL SECTION

Device Fabrication. Detailed experimental description is shown in Figure S1. First, monolayer graphene was grown on polished Ge(110) substrates (ingot no.: GH221, AXT) by CVD using conditions that had been optimized as described previously.[11] As-grown Gr on Ge(110) was loaded in an ultrahigh vacuum (~10^{-6} Torr) chamber, and then thermally evaporated metal (= Al, Cr, Cu, Ni, or Au) was deposited onto Gr and then capped with a 30 nm thick Au layer. After Al was deposited on Gr, 5 nm Cr were deposited to achieve good adhesion between Al and Au layers. For Pt, e-beam evaporator was used to deposit a 40 nm-thick Pt layer onto Gr. Then PMMA (996 K, 8% in anisole) was spin-coated on the metallized Gr/Ge at 3000 rpm for 100 s and then annealed at 180 °C for 10 min on a hot plate. When the metal used was prone to oxidation, the annealing procedure was conducted in a glovebox in N_2 atmosphere. To exfoliate PMMA/M/Gr from Ge substrate, thermal release tape (TRT) was attached and then detached. Then the PMMA/M/Gr stacks on the TRT were reattached to *n*-type (10^{15} cm^{-3} of phosphorus dopants) Si substrates (Si(111) - part no.: PWNT05525-5P, LG Siltron Inc., Si(100) - lot no.: 0505-81003-001, STC), which had been precleaned right before the reattachment (within 30s) to minimize air-born contamination. The Si(111) substrates were cleaned by sonication for 10 min in acetone and then dipped in boiling DI water for 20 min and in piranha solution for 10 min. After that, the Si(111) substrates were treated with 40 wt % NH_4F aqueous solution (product code: 64025S0401, JUNSEI) for 10 min.[32] The Si(100) substrates were treated with buffered oxide etchant (NH_4F:HF = 6:1) (product number: 901624−1L, Sigma-Aldrich) for 50 s. The TRT was released at 130 °C on a hot plate, then the PMMA was removed using O_2 plasma (120 W, 15 min). The back of the Si surface was contacted by thermally evaporated 10 nm Al/5 nm Cr/30 nm Au after scratching the surface with a diamond cutter. Finally, the devices were postannealed at 240 °C in low-pressure (~10^{-1} Torr) H_2 atmosphere for 4 h. The junctions in Figure S4a were exposed to chloroform for 15 min instead of O_2 plasma during fabrication.

The Au/Gr/Si device array was fabricated using conventional lithography techniques. First, an Au/Gr/Si(100) junction was prepared as described. PMMA was removed by chloroform. Then photoresists (DNR L-300) were patterned as 22 μm × 22 μm squares on the Au surface. Then Au etchant (product no. 651818-500 ML, Sigma-Aldrich) was used to etch away the uncovered Au. O_2 plasma was used to remove the uncovered Gr, then photoresists were removed using acetone. Then 600 nm SiO_2 was deposited on the sample by plasma enhanced CVD (Instrument model: HiDep-SC, BMR Technology). The photoresist (SU-8 2000) was coated with 13 μm × 13 μm holes on prepatterned Au/Gr square array under SiO_2. The sample was etched by inductively coupled plasma (ICP) and dipped in BOE to remove SiO_2 from the prepatterned holes. The photoresist was removed, and then Cu electrodes were thermally deposited on patterned holes through a shadow mask.

M/Si junctions were fabricated by thermal deposition of 40 nm thick metals with 300 μm × 300 μm squares through a shadow mask on the same Si substrates.

Work Function Characterization. $W_{Gr/M}$ was obtained by UPS (instrument model: ESCALAB 250Xi, Thermo Scientific) with monochromated He I radiation ($h\nu$ = 21.2 eV). Measurements were conducted on TRT-supported PMMA/M/Gr surfaces, which had been detached from the Ge substrate right before being mounted in the UPS chamber. Carbon tape was used to connect the Gr surface to photocurrent circuits in the UPS instrument. The kinetic energy E_k of emitted electrons was collected as a relative intensity profile. Bound energy (B.E.) was calculated as B.E. = $h\nu - E_k$, and the maximum value of measured B.E. was defined as the intersection point of an offset line and an initial slope line near the maximum B.E. (Figure 2a). $W_{Gr/M}$ was determined as $h\nu$ − (maximum measured B.E.). W_M for pure metals were obtained from the literature.[33]

Electrical Characterization. *J*−*V* measurements were conducted using a probe station in a dark shield box (instrument model: MST5500B, MS TECH). Two-point probing was conducted on fabricated M/Gr/Si devices by setting one probe contact on the M/Gr pad as the drain point (voltage applied) and the other probe contact on the back of the Si as the source point (grounded). *J* was calculated by dividing the measured current by covered M/Gr area in an optical image. Schottky barriers were obtained by fitting *J*−*V* data using the TE model[1]

$$J^{TE} = A^*T^2 \exp\left(-\frac{e\Phi_B}{kT}\right)\left(\exp\left(\frac{eV}{\eta kT}\right) - 1\right)$$

where $A^*$is the Richardson constant, assumed to be 112 A/(K^2·cm^2), which is a theoretical value for *n*-Si at rt.[1] $k = 8.617 \times 10^{-5}$ eV/K is the Boltzmann constant, T = 300 K, and $e = 1.602 \times 10^{-19}$ C is the elementary charge. We used $e\Phi_B$ and η as variables for curve-fitting.

TEM Sample Fabrication and Characterization. For TEM cross-sectional imaging, Au/Gr/Si(111) and Au/Gr/Si(100) devices were prepared as described. *J*−*V* data (Figure 4) were collected from the devices before TEM sampling. Cross sections of the devices were prepared using a focused ion beam (instrument: Helios NanoLab G3 CX, FEI) after deposition of a protective carbon layer (1.7 μm). Then it was mounted at a side of a copper lift-out grid and subjected to final milling at 1−2 kV. TEM imaging was conducted (instrument: ARM-200F, JEOL) with fifth-order spherical aberration corrector (instrument: ASCOR, CEOS GmbH) at acceleration voltage = 200 kV. For STEM imaging, ABF mode was used with a 50-μm condenser lens aperture and 10 cm camera length at acceleration voltage = 200 kV.

XPS Sample Fabrication and Characterization. For the fabrication of XPS samples, the Au/Gr bilayer was transferred on Si(111), followed by Au etching. Then 1.5 nm thick Au was evaporated onto the Gr/Si(111) surfaces, together with bare Si(111) surfaces in an ultrahigh vacuum (~10^{-6} Torr) chamber. XPS measurements (instrument model: ESCALAB 250Xi, Thermo Scientific) were conducted on both Au/Gr/Si(111) and Au/Si(111) surfaces with an Al Kα X-ray source ($h\nu$ = 1486.6 eV).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.1c03299.

Schematics of the steps to fabricate M/Gr/Si junction devices, optical images of M/Gr/Si, Raman mapping data from Gr, STEM image of Au/Gr/Si(111), line intensity profile of Au on HRTEM image of Au/Gr/Si(111), *J*−*V* characteristics of M/Gr/Si(100) with wet process conditions, optical image of Au/Gr/Si junction arrays with *J*−*V* characteristics, circuit diagram for M/Gr/Si junction devices, HRTEM image of Au/Gr/Si(100), and XPS data of Au/Si and Au/Gr/Si interface (PDF)

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Author Contributions

†J.-H.P. and S.-J.Y. contributed equally to this work. J.-H.P., S.-J.Y., and C.-J.K. designed the experiments. S.-J.Y. grew graphene samples. C.-W.C. and S.-Y.C performed the HRTEM and STEM imaging. C.-J.K. and J.-H.P. carried out electrical measurements and data analysis. C.-J.K., S.-J.Y., and J.-H.P. conducted the sample fabrication and optical characterization, and wrote the manuscript with input from all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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